WHAT IS CLAIMED IS:

1. A system for generating multiple drive strengths for one or more output signals of a memory controller, the memory controller operable to control a memory subsystem, the system comprising:

a state machine operable to generate an n-bit output representative of a drive strength operable to drive the one or more output signals; and

a plurality of adders, each adder having a plurality of n-bit inputs, each input receiving a selective set of bits from the n-bit output of the state machine, the plurality of adders generating a plurality of n-bit outputs representative of a plurality of drive strengths operable to drive the one or more output signals.

2. The system of claim 1, wherein the plurality of adders are operable to generate the plurality of n-bit outputs in increments of less than or equal to 0.25 times a drive strength required by a motherboard operatively coupled to the memory subsystem.

3. The system of claim 1, the plurality of adders operable to generate the plurality of n-bit outputs in increments of less than or equal to 0.5 times a drive strength required by a motherboard operatively coupled to the memory subsystem.

4. The system of claim 1, wherein the state machine is a RCOMP state machine operable to generate the n-bit output representative of the drive strength.

5. The system of claim 1, further comprising:

a control register configured to store one or more control words representative of a loading on a pin of a memory organization of the memory subsystem; and

one or more multiplexers configured to receive the plurality of n-bit outputs from the plurality of adders, the n-bit output from the state machine, and shifted values of the n-bit output from the state machine, the one or more multiplexers operable to select as an operating drive strength, based on the one or more control words, one of the plurality of n-bit outputs from the plurality of adders, the n-bit output from the state machine, or one of the shifted values of the n-bit output from the state machine.

6. The system of claim 5, further comprising:

one or more output drivers operable to drive the one or more output signals; and

one or more decoders configured to receive the operating drive strength from one of the one or more multiplexers, the one or more decoders operable to adjust the one or more output drivers to operate at the operating drive strength.

7. The system of claim 6, further comprising:

one or more selectors, each selector coupled between two or more multiplexers and one or more decoders, the one or more selectors configured to receive two or more operating drive strengths from the two or more multiplexers, and operable to selectively couple one of the two or more operating drive strengths to the one or more decoders.

8. The system of claim 7, further comprising:

a storage element configured to store a memory value representative of the type of memory contained in the memory organization, the selectors operable to selectively couple one of the two or more operating drive strengths to the one or more decoders based on the memory value.

9. The system of claim 8, wherein the memory value is a binary number representing either synchronous dynamic random access memory (SDRAM) or double data rate (DDR) memory.

10. The system of claim 5, the control register configured to store one or more 3-bit control words representative of the loading on the pin of the memory organization.

11. The system of claim 7, wherein the plurality of adders are operable to generate the plurality of n-bit outputs in increments of less than or equal to 0.25 times a drive strength required by a motherboard operatively coupled to the memory subsystem.

12. The system of claim 7, the plurality of adders operable to generate the plurality of n-bit outputs in increments of less than or equal to 0.5 times a drive strength required by a motherboard operatively coupled to the memory subsystem.

13. A system comprising:

a memory subsystem with a memory organization containing a memory device; and

a memory controller operable to provide one or more output signals, the one or more output signals operatively

coupled to the memory subsystem, the memory controller comprising:

a state machine operable to generate an n-bit output representative of a drive strength operable to drive the one or more output signals; and

a plurality of adders, each adder having a plurality of n-bit inputs, each input receiving a selective set of bits from the n-bit output of the state machine, the plurality of adders generating a plurality of n-bit outputs representative of a plurality of drive strengths operable to drive the one or more output signals.

14. The system of claim 13, the memory controller further comprising:

a control register configured to store one or more control words; and

one or more multiplexers configured to receive the plurality of n-bit outputs from the plurality of adders, the n-bit output from the state machine, and shifted values of the n-bit output from the state machine, the one or more multiplexers operable to select as an operating drive strength, based on the one or more control words, one of the plurality of n-bit outputs from the plurality of adders, the n-bit output from the state machine, or one of the shifted values of the n-bit output from the state machine.

15. The system of claim 14, further comprising:

a processor operable to execute a routine, the routine operable to determine a loading on one or more pins of the memory organization and to program in the control register one

or more n-bit control words representative of the loading on the one or more pins.

16. The system of claim 15, the routine operable to program in the control register one or more 3-bit control words representative of the loading on the one or more pins.

17. The system of claim 15, the memory controller further comprising:

one or more output drivers operable to drive the one or more output signals; and

one or more decoders configured to receive the operating drive strength from one of the one or more multiplexers, the one or more decoders operable to adjust the one or more output drivers to operate at the operating drive strength.

18. The system of claim 17, the memory controller further comprising:

one or more selectors, each selector coupled between two or more multiplexers and one or more decoders, the one or more selectors configured to receive two or more operating drive strengths from the two or more multiplexers, and operable to selectively couple one of the two or more operating drive strengths to the one or more decoders.

19. The system of claim 18, the memory controller further comprising:

a storage element configured to store a memory value representative of the type of memory contained in the memory organization, the selectors operable to selectively couple one of the two or more operating drive strengths to the one or more decoders based on the memory value.

20. The system of claim 19, wherein the memory value is a binary number representing either synchronous dynamic random access memory (SDRAM) or double data rate (DDR) memory.

21. The system of claim 17, the memory organization including a double in-line memory module (DIMM) containing a nonvolatile memory (NVRAM) configured according to a serial presence detect protocol.

22. A method for generating multiple drive strengths for an output signal of a memory controller, the memory controller operable to control a memory subsystem, the method comprising:

generating an n-bit output representative of a drive strength operable to drive the output signal; and

adding combinations of two or more selective sets of bits from the n-bit output to generate a plurality of n-bit outputs representative of a plurality of drive strengths operable to drive the output signal.

23. The method of claim 22, comprising adding combinations of the two or more selective sets of bits from the n-bit output to generate a plurality of n-bit drive strengths in increments of less than or equal to 0.25 times a drive strength required by a motherboard operatively coupled to the memory subsystem.

24. The method of claim 22, comprising adding combinations of the two or more selective sets of bits from the n-bit output to generate a plurality of n-bit drive strengths in increments of less than or equal to 0.5 times a drive strength required by a motherboard operatively coupled to the memory subsystem.

25. A method for controlling a memory subsystem having a memory organization in a system comprising:

determining a loading on a pin of the memory organization;

generating an n-bit output representative of a drive strength;

adding combinations of two or more selective sets of bits from the n-bit output to generate a plurality of n-bit outputs representative of a plurality of drive strengths; and

adjusting an output driver of a memory controller operatively coupled to the memory subsystem to operate at one of the generated n-bit drive strengths based on the loading.

26. The method of claim 25, the determining step includes accessing a predetermined storage element in the memory subsystem to retrieve information pertaining to the loading on the pin of the memory organization.